S/N 09/652,430 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Biswajit Sur et al.	Examiner: Andy Huynh
Serial No.:	09/652,430	Group Art Unit: 2818
Filed:	August 31, 2000	Docket No.: 884.319US1
Title:	ELECTRONIC ASSEMBLY COMPRISING SOLDERABLE THERMAL INTERFACE (As Amended)	
Customer No:	21186	Assignee: Intel Corporation

DECLARATION UNDER 37 C.F.R. § 1.131

Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

This declaration is submitted under 37 C.F.R. §1.131 prior to any final rejection of U. S. Patent Application Serial Number 09/652,430 to establish invention of the subject matter of the rejected claims prior to September 30, 1999.

I, Biswajit Sur, do hereby declare:

1. I have been employed by Intel Corporation from prior to September 30, 1999 until the present. My current job title is Manager of Assembly and Packaging.

2. I am a co-inventor of the inventive subject matter of the present application as described illustrated, and claimed therein.

3. Prior to September 30, 1999, the inventive subject matter that is described, illustrated, and claimed in corresponding claims of the present application was completed in the United States as evidenced by the following:

a. Prior to September 30, 1999, having earlier conceived the claimed subject matter in the United States with the co-inventors, I personally generated an Invention Disclosure, a copy of which is attached hereto as Exhibit A (7 pages). The "Invention Date" deleted from page 1 of Exhibit A is prior to September 30, 1999. Other sensitive information has been blocked out from Exhibit A.

b. Figure 1 of Exhibit A illustrates conceptually an integrated circuit die attached to an organic land grid array (OLGA) substrate with solder bumps. An integrated heat spreader (IHS) is attached to the back side of the die using a low melting point solder-based thermally conductive interface material, also referred to variously in Exhibit A as "thermal interface material", a "thermal attach", and a "thermal interface".

c. Prior to September 30, 1999, I was personally involved in the construction of prototype integrated circuit packages utilizing a solder thermal interface technique, as described in Exhibit A. My responsibilities included the design, selection, and procurement of low melting point solder materials/alloys; plating of solderable metal layers on lids; defining a suitable and manufacturable process to form a reliable thermal interface between the integrated circuit device and the lid compatible with the package and circuitry; building and testing of prototypes; and analyzing the results.

d. The results of four different low melting point solder alloys tested are shown in Table 2 of Exhibit A. These solder alloys (Cu_2, Cu_281, Cu_290, and Cu_4) correspond to the four solder alloys identified by the corresponding Indalloy numbers in Table 1 on page 9 of the present application.

e. Prior to September 30, 1999, I generated a Powerpoint presentation entitled "Results from Experiments on Solder Alloy as Thermal Interface Material", which summarizes the results of experiments using a low melting point solder alloy as a thermally conductive interface material. Pages 1-4 of this Powerpoint file are attached hereto as Exhibit B (4 pages). The date deleted from the footer of Exhibit B is prior to September 30, 1999. Other sensitive information has been blocked out from Exhibit B.

f. Exhibit B, page 2, describes forming successive layers of titanium (Ti), nickel-vanadium (Ni/V), and gold (Au) on the backside of a die; coating two different types of heat spreaders, one made of aluminum-silicon-carbide (AlSiC) and the other made of

copper (Cu), with nickel (Ni); and testing four different low melting point solder materials identified by Indalloy Numbers 281, 290, 2, and 4. Again, these solder alloys correspond to the four solder alloys identified by corresponding Indalloy numbers in Table 1 on page 9 of the present application, and they also correspond to the four solder alloys appearing in Table 2 of Exhibit A.

g. Exhibit B, page 3, describes various assembly details in forming prototype integrated circuit packages incorporating a low melting point solder alloy as a thermally conductive interface material.

h. Exhibit B, page 4, illustrates a graph of thermal resistance measurements for eight different prototype integrated circuit packages incorporating a low melting point solder alloy as a thermally conductive interface material.

i. When I finished testing and evaluating the prototype integrated circuit packages believed that they worked satisfactorily for their intended purpose, i.e. to transfer heat from an integrated circuit through a low melting point solder-based thermal interface material to a lid or integrated heat spreader.

4. I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements are made with the knowledge that willful false statements and the like are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of this application or any patent issuing thereon.

Date: 9-11-2003

Biswajit Sur

DECLARATION UNDER 37 C.F.R. § 1.131
Serial Number: 09/652,430
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Assignee: Intel Corporation

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Dkt: 884.319US1 (INTEL)

BISWAJIT SUR ET AL.

By their Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
Attorneys for Intel Corporation

Date 9/12/2003

By _____
Walter W. Nielsen
Reg. No. 25,539

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this ____ day of September, 2003.

Name

Signature

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INVENTION DISCLOSURE, Rev 1
Located at: http://legal.intel.com

[redacted]

LEGAL ID# _____(legal dept. use only) DATE: Invention Date

It is important to provide accurate and detailed information on this form (fill in ALL areas under Inventor[s]). The information will be used to evaluate your invention for possible filing as a patent application. When completed, please return this form to Janice Boulden, Intel Legal Department at JF3-147. You can submit electronically if all of the information is electronic, including drawings and supervisor approval. If you have any questions regarding this form or to whom it should be forwarded, please call 503-264-0444.

Fill out the below and follow the instructions:

1. Field of the Invention:

Semiconductor Process: device and integration
Semiconductor Process + Equipment: thin films
Semiconductor Process + Equipment: etch/litho
Circuit Design
Flash
Test
CON (GMT)
X Packaging
Boards/Cartridge
Automation
Other

RECEIVED
PATENT DATABASE GROUP
INTEL LEGAL TEAM

2. Concise Title of Invention:

A low-melting soft solder thermal interface technique for organic flip-chip packages to dissipate a high power density.

3. Brief Description of Invention (please use only space provided and font #10 or larger. Write the Key Elements of the Invention):

The Invention is: Technique of forming a high performance thermal interface using a low-melting soft solder alloy between the flipped die and the integrated heat spreader in an organic flip-chip package (also known as C4 OLGA). The proposed thermal interface will have a capability of dissipating a large power density. Quantitatively, this interface will provide a thermal resistance that is (at least) twice as good as compared to the best available polymeric thermal interface of today. The added advantage of this specific low-melting soft solder approach is that it is not expected to negatively degrade the package reliability.

Description:

Problem: Today's best available polymeric thermal interface materials (silver filled or aluminum filled) are capable of delivering a normalized thermal resistance of 0.4°C-cm^2/W for a large die, and a target of 0.30°C-cm^2/W is considered to be a stretch goal.

Solution: In order to break the thermal resistance barrier a high performance thermal interface is required. An inherent high thermal conductivity, and a proper bondline control are the two elements in achieving such a high performance interface. Using the proposed technique of this disclosure a low melting point soft solder alloy of high thermal conductivity can be used as the thermal interface. The proper adhesion and bondline control of the interface are be achieved by a proper selection of solderable interfaces, and process conditions.

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4. Inventor(s):

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Citizenship: India	Supervisor Name: Kevin J. Haley	Supervisor Phone: 408-765-4062	Supervisor M/S: SC12-504
Group Name: IPD	BUM Presenter: Steve Smith	Inventor Signature: Biswajit Sur	
Division Name: ATD___ PTD___ CTM___ CR___ STTD___ OQN ___ SMTD____TCAD___ Other?___MPSI_____			
Name: Nagesh Vodrahalli	SS#	Empl.#	M/S: CH5-185
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Group Name: TMG	BUM Presenter:	Inventor Signature:	
Division Name: ATD___ PTD___ CTM___ CR___ STTD___ OQN ___ SMTD____TCAD___ Other?_____			
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Phone: (408) 653-8051	Fax: (408) 765-7798		
Citizenship: USA	Supervisor Name: Jim Hendrix	Supervisor Phone: (408) 766-9690	Supervisor M/S: RN2-35
Group Name: DI project	BUM Presenter: Ed So	Inventor Signature:	
Division Name: ATD___ PTD___ CTM_X__ CR___ STTD___ OQN ___ SMTD____TCAD___ Other?_____			

(PROVIDE SAME INFORMATION AS ABOVE FOR EACH ADDITIONAL INVENTOR)

5. ***HAVE YOUR SUPERVISOR READ, DATE AND SIGN COMPLETED FORM (use first inventor's supervisor if multiple inventors)***

DATE:_____ **SUPERVISOR NAME:** Kevin Haley

BY THIS SIGNING, I (SUPERVISOR) ACKNOWLEDGE THAT I HAVE READ AND UNDERSTAND THIS DISCLOSURE, AND RECOMMEND THAT THE HONORARIUM BE PAID.

EXHIBIT A - Page 2

4. Inventor(s):

Name: Biswajit Sur Phone: 408-786-5738 Citizenship: India Group Name: ECI Division Name: ATR___ FTE___ GTM___ GR___ STTR___ OSN___ SMTD___TOAR___ Other?___MDB___	Fax: 408-[illegible] Supervisor Name: Kevin J. Haley SLIM Presenter: Steve Smith	Empl.#	MS: EC13-604
		Supervisor Phone: 408-786-4082 Inventor Signature:	Supervisor MS: EC13-604
Name: Nagesh Vedanketi Phone: 402-554-5001 Citizenship: USA Group Name: TIMS Division Name: ATD___ FTE___ GTM___ GR___ STTR___ OSN___ SMTD___TOAR___ Other?_____	Fax: 402-536-4091 Supervisor Name: Fiona Stubbs SLIM Presenter:	Empl.#	MS: CH5-166
		Supervisor Phone: 408-786-[illegible] Inventor Signature:	Supervisor MS: [illegible]
Name: Tom Weakman Phone: (408) 863-6051 Citizenship: USA Group Name: [illegible] Division Name: ATD___ FTE___ GTM_X__ GR___ STTR___ OSN___ SMTD___TOAR___ Other?_____	Fax: (408) 786-77[illegible] Supervisor Name: Jim Hendrix SLIM Presenter: Ed Su	Empl.#	MS: RN2-66
		Supervisor Phone: (408) 786-6000 Inventor Signature:	Supervisor MS: RN2-66

[PROVIDE SAME INFORMATION AS ABOVE FOR EACH ADDITIONAL INVENTOR]

5. *HAVE YOUR SUPERVISOR READ, DATE AND SIGN COMPLETED FORM (see first Inventor's supervisor if multiple inventors)*

DATE: _____ SUPERVISOR NAME: _____

BY THIS SIGNING, I (SUPERVISOR) ACKNOWLEDGE THAT I HAVE READ AND UNDERSTAND THIS DISCLOSURE, AND RECOMMEND THAT THE HONORARIUM BE PAID.

4. Inventor(s):

Name: Shrenik Sor Phone: 408-705-6738 Citizenship: India Group Name: ED Division Name: ATD___ PTD___ CTH___ CR___ STTD___ CON___ SMTL___ TOAD___ Other?___ SER___	Site Fax: 408-[illegible] Supervisor Name: Kevin J. Malloy SUM Preparer: Steve Sorkin	Empl.#	MS SC10-604 Supervisor Phone: 408-[illegible] Supervisor MS: SC10-604 Inventor Signature:
Name: (Nagesh Vashishth) Phone: 408-864-xxxx Citizenship: USA Group Name: TMM Division Name: ATD___ PTD___ CTH___ CR___ STTD___ CON___ SMTL___ TOAD___ Other?___	Site Fax: 408-[illegible] Supervisor Name: Ramin Shokin SUM Preparer:	Empl.#	MS: CH5-165 Supervisor Phone: 408-765-6919 Inventor Signature:
Name: Tom Wortmann Phone: (xxx) xxx-xxxx Citizenship: USA Group Name: [illegible] Division Name: ATD___ PTD___ CTH_X__ CR___ STTD___ CON___ SMTL___ TOAD___ Other?___	Site Fax: (408) 765-7758 Supervisor Name: Jim Hendrix SUM Preparer: [illegible]	Empl.#	MS RN5-55 Supervisor Phone: (408) 765-[illegible] Inventor Signature: Th N. Wo Supervisor MS: RN5-55

[illegible] SAME INFORMATION AS ABOVE FOR EACH ADDITIONAL INVENTOR)

6. *HAVE YOUR SUPERVISOR READ, SIGN AND SIGN COMPLETED FORM (see first inventor's supervisor if multiple inventors)*

DATE: _____ SUPERVISOR NAME: _____

BY THIS SIGNING, I (SUPERVISOR) ACKNOWLEDGE THAT I HAVE READ AND UNDERSTAND THIS DISCLOSURE, AND RECOMMEND THAT THE HONORARIUM BE PAID.

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Rev 1, 2/98

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TOTAL P.02

TOTAL P.02

EXHIBIT A - Page 4

6. Has subject matter of present disclosure been disclosed or will it be disclosed outside Intel?
If yes, explain and give date: No. But outsiders can determine the technique by cross-sectioning a package. The earliest implementation of this technique in a package can be
(Give expected tape out date if applicable):

7. Has the subject matter of present disclosure been published or will it be published outside of Intel? Not planned currently.
If yes, explain and give date:

8. Has a product using or manufactured using the present disclosure been sold or offered for sale?
If yes, explain and give date: If successful, will be used in future products. Earliest

9. Has this invention been conceived, or constructed during accomplishment of a government or third party contract? If yes, give contract name and number: N/A

10. Explain the problem being addressed by the invention:

This invention addresses the problem of:

Today's best available polymeric thermal interface materials (silver filled or aluminum filled) are capable of delivering a normalized thermal resistance of 0.4°C-cm^2/W for a large die.

Moreover, many polymeric materials also produce inherent process artifacts, such as, resin separation, out-gassing, spreader to die delamination, pump-out, etc.

11. Explain current state of the art (i.e. how the problem is solved today):

Presently the problem described above is solved by:

A stretch goal of 0.3°C-cm^2/W is anticipated today using a polymeric material as thermal interface of a large die, and any further improvement is assumed not achievable.

12. Explain technical advantages of the invention over current state of the art:

The technical advantage of this invention is:

The proposed utilization of a highly conductive solder alloy will provide a thermal resistance that is (at least) twice as good as compared to the best available polymeric thermal interface of today. Moreover, the utilization of a soft solder is to keep package and die level stresses low. The choice of a low-melting point is to attain a relatively lower processing temperature and thereby reducing warpage induced stress in the system. The above two conditions are intended to reduce total stress level in an OLGA2 package and thereby enhance the package reliability.

13. a. Is the invention experimentally verified? Yes.
b. Is the invention verified with simulation? No.
c. If neither a. or b. above, then you can get a patent on the concept, but please explain the technical basis to justify that your invention will work (use extra space if necessary):

Please check next section for experimental verification.

14. **Detailed Description of Invention (try to use only the space provided with font #10 or larger type. Refer to your drawings).**

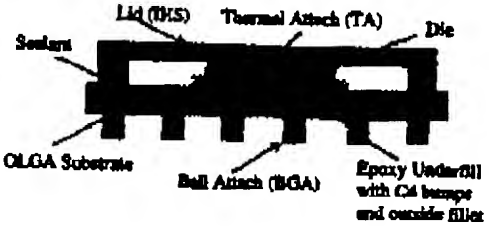


Figure 1. Schematic of an OLGA2 package showing the backside of die attached to IHS with the help of thermal interface material.

As a background, an OLGA2 package consists of a flip-chip silicon die attached to an organic land grid array (OLGA) substrate with the help of C4 bumps and an underfill epoxy. An integrated heat spreader (IHS) is attached to the backside of the flip-chip die for heat dissipation. A thermally conductive interface (which is the topic of this disclosure) is used to attach the IHS to the die. IHS is also attached to the substrate boundary with the help of a sealant for mechanical support. Various components of an OLGA2 package, including the thermal interface / thermal attach are schematically shown in Figure 1.

For forming a low-melting soft solder thermal interface the following four components are essential: 1) a solderable die backside, 2) a solderable IHS, 3) a suitable solder paste, and 4) a suitable process for forming a reliable interface. A procedure for achieving the above four is described in the following.

1) Firstly metal layers are required to be deposited on the backside of die (unpolished wafer) for solderability. The backside of an unpolished wafer is prepared with a 10 second sputter etch before the metal deposition/sputtering. The metal layer build-up is as follows: a 500Å layer of Ti on backside of the die, followed by a 3500Å layer of Ni/V, and finally a 600Å layer of Au. The sputtering parameters are similar to that used for POR C4 BLM processing (C4 BLM Ti, C4 BLM Ni/V), with the addition a gold layer with a P6 backside Au-parameters (except for shorter deposition time). Test wafers of 2C112M45 device were used for this test.

2) Solderability on IHS can be achieved with a presence of a suitable metal. Two types of IHS materials (Cu and AlSiC) were tried in this feasibility test. A 2 to 5 µm thick Ni layer with shiny finish was found suitable for attaining solderability on both the material types. Electroless Ni plating was done in a Nikitel 787 bath, using a medium force solution.

3) Several different solder alloys (Bi or In alloy) were tried out and found suitable for this thermal interface application. All of them were off-the-shelf materials from Indalloy Corp, and were available in solder paste form. The solder paste consists of a no-clean flux vehicle and a 88% loading of the corresponding solder alloy. The solder compositions and relevant properties are given in the following Table 1.

Table 1. Compositions and relevant properties of the solder alloys used in this experiment.

Indalloy Number	Composition	Liquidus (°C)	Solidus (°C)	Thermal Conductivity (W/m*°C)
281	58 Bi / 42 Sn	138	138	19
290	57 In / 3 Ag	143	143	73
9	50 In / 15 Pb / 5 Ag	154	149	46
4	100 In	157	MP	86

4) During assembly process the solder paste is first applied at backside of die, and then the sealant material is dispensed on the package boundary. The IHS is then placed, and IHS spring is attached to apply a 3 to 5 lbs of force. The units in a FOL carrier are then reflowed in N2 environment inside a horizontal BTU furnace for forming the solder joints. During reflow operation of each alloy, the maximum zone temperature in the furnace was maintained at 'liquidus + 30°C' and the time above liquidus was ~60 secs. Post solder join the sealant was cured in a conventional vertical oven.

15.

Drawings (use as many pages as needed)
(PLEASE DO NOT MAKE COLOR DRAWINGS)

16. **Key Supporting Data (1 page limit on separate page):**

The experimental feasibility of this technique is shown in the following figures. The thermal resistance data from 4 alloys were referred to by their numbers and by the type of spreaders (for example, Cu_2 means Cu spreader with indalloy#2 combination). Only the data for Cu IHS is demonstrated here.

Figure 2. Comparison of thermal interface resistance (°C-cm²/W) between all the alloys tested and the present plan of record material. Data shown are for the center sensor (RTD3) for a 2C11ZL die (884x904 mils)

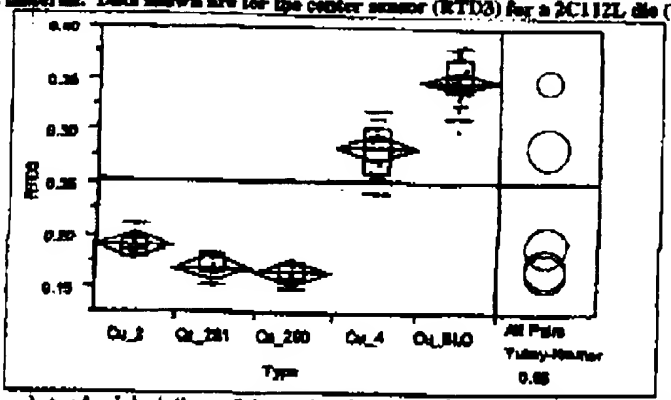
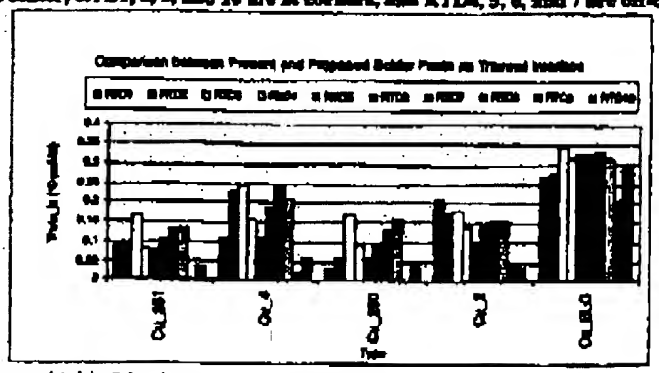


Table 2. Mean and standard deviations of thermal resistance at die center for all legs tested.

Means and Std Deviations

Level	Number	Mean	Std Dev	Std Err Mean
Cu_2	7	0.160	0.011	0.004
Cu_281	7	0.169	0.010	0.004
Cu_280	7	0.185	0.008	0.003
Cu_4	7	0.236	0.026	0.010
Cu_BLO	16	0.349	0.022	0.006

Figure 3. Thermal resistance for all the temperature sensors for all the legs (only 1 unit per leg shown). RTD3 and 8 are at center, RTD1, 2, 9, and 10 are at corners, and RTD4, 5, 6, and 7 are off-centered in the die.



From above figures and table it is clear that the proposed solder thermal interface technique outperformed the present POR interface, both statistically and technically, by a vast margin (Fig. 1 and Table 2). This improvement is noticed uniformly all across the die, as can be seen for all the sensors (Fig. 3). It is to be also noted that, without any process optimization, this proof of concept test already showed about a 2X improvement in thermal performance.

Results from Experiment on Solder Alloy as Thermal Interface Material

B. Sur, T. Workman

Build Details

- 2C112L device was used for this investigation
- Metal was sputtered on backside of die (wafer) for solderability
  - Wafers did not have any backside polishing step
  - Metal sputtering on backside at D2: 500Å Ti + 3500Å Ni/V + 600Å Au

- AlSiC (CPS) spreaders were coated with Ni plating
  - Ni plating (electroless) at a Santa Clara shop

- Cu (Shinko) spreaders had POR Ni coating
- Four (4) 'off-the-shelf' solder pastes used as thermal interface material
  - Solder paste supplier: Indium Corporation of America

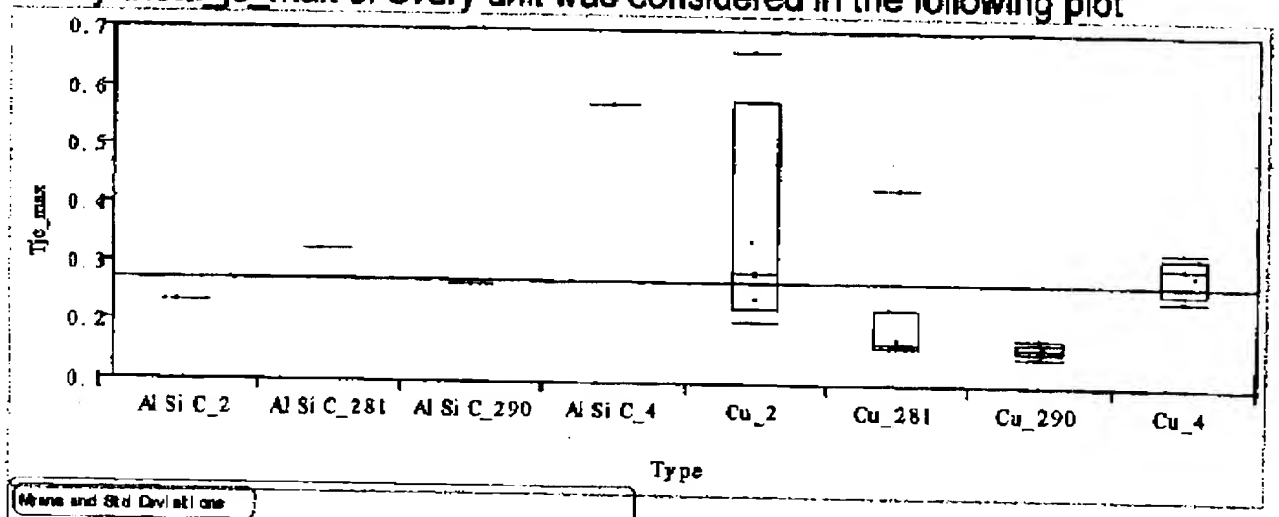
Indalloy Number	Composition	Liquidus (°C)	Solidus (°C)	Thermal Conductivity (W/m-°C)
281	58 Bi / 42 Sn	138	138	19
290	97 In / 3 Ag	143	143	73
2	80 In / 15 Pb /	154	149	43
4	100 In	157	MP	86

Build Details (Contd.)

- IHS Assembly Details:
  1) Solder paste manually applied at backside of die
  2) Sealant dispensed on package
  3) Spreader placed using manual SPM and template
  4) IHS springs attached
     IHS spring used:
  5) Reflowed in chip-join BTU furnace for solder joint of thermal interface
     Belt speed:
     Temperatures:
     Environment:
  6) Cured

Tjc_max for all the Units

- Thermal resistance is normalized for die area (°C-cm²/W)
- Only theta_jc_max of every unit was considered in the following plot



Means and Std Deviations

Level	Number	Mean	Std Dev	Std Err Mean
Al Si C_2	1	0.233	?	
Al Si C_281	1	0.324	?	
Al Si C_290	1	0.267	?	
Al Si C_4	1	0.577	?	
Cu_2	7	0.365	0.184	0.0
Cu_281	7	0.215	0.099	0.0
Cu_290	7	0.166	0.011	0.0
Cu_4	7	0.294	0.030	0.0

Summary:

- **Results show proof-of-concept that 'solder' thermal interface can give a very low thermal resistance. For example: (lot_μ+3*lot_σ) for (Cu+Alloy290) = 0.199 °C-cm²/W**